REMARKS

I. Summary of Office Action

Claims 1-6 were pending with Claim 1 being independent.

On May 18, 2007, the Patent Office mailed a non-final Office Action in which the Examiner objected to claims 1-6 under 37 C.F.R. § 1.75 for informalities such as the use of acronyms and unclear use of terms.

Claims 1-3,5 and 6 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Schaeffer, JR. *et al.* U.S. Patent Application PG Pub US 2003/0062990 A1 ("Schaeffer).

Claim 4 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious from Schaeffer, JR. *et al.* U.S. Patent Application PG Pub US 2003/0062990 A1 ("Schaeffer), in view of Ashlock et al (PG Pub US 2002/0095662 A1)

II. Summary of Applicants' Response

Applicants have amended claims 1-6 to clarify names of the elements per the specification, spell out acronyms and replace the slash mark with the word "and" in order to address the Examiner's objections.

Applicants also have amended independent claim 1 with a clarification of the subsystem names. No new matter has been added.

Applicants have also amended dependent claims 2-6 with similar clarifications. No new matter has been added.

The Examiner is respectfully requested to withdraw the rejections under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) in view of the following remarks.

III. Claim Objections

Regarding Claims 1, 3-6, the examiner made several suggestions for clarity. The claims have been amended to spell out Acronyms upon its first usage in a set of claims. For example, in Claim 1, "MAC/PHY layer" is replaced with "Medium Access Control and Physical Layer (MAC and PHY)", and in Claims 3, PLC in Line 2 is replaced by " Power Line Communications (PLC)".

Regarding Claim 1, 3-6, the forward slash in MAC/PHY and MDU/MTU has also been replaced with the word "and".

Regarding Claim 1, it was unclear that "the programmable coprocessor modules" in Line 3-4, is intended to be the same as or different from the limitation "programmable pre-defined operation hardware coprocessor module" recited in Line 1-2. They are different. The first reference is for the entire module and the second refers to its parts, Claim 1 was amended to reflect the terms in the specification and clarify that the hardware blocks, coprocessor and some of the PHY functions are part of the controller that is connected to a general purpose processor and DSP logic. The first term will be "the programmable pre-defined operation hardware coprocessor modules". The second term will be amended to include "controls pre-defined hardware blocks having parameterized functions whose parameter values are programmable"

Regarding Claim 2, it was unclear whether the limitation "the hardware module" in Line 1 is intended to be the same or different from the limitation "programmable predefined operation hardware coprocessor modules" recited in Claim 1, line 1-2. The "hardware module" will be amended to "programmable pre-defined operation hardware coprocessor modules"

Regarding Claim 3-6, it was unclear whether "the hardware modules" in Line 1, respectively, is intended to be the same or different from the limitation "programmable pre-defined operation hardware coprocessor modules" recited in Claim 1, line 1-2. The "hardware module" will be amended to "programmable pre-defined operation hardware coprocessor modules"

IV. 35 U.S.C. § 102(b)

Regarding the 35 U.S.C § 102(b) rejections in section 3 as a result of being anticipated by Schaeffer, JR. et al (PG Pub US 2003/0062990 A1) the Applicants make the general clarification, followed by responses to the rejections.

The MAC and the PHY in high-speed communication systems are often thought of in two ways: a logical perspective, which describes the functions the MAC performs, and a physical perspective which describes how it is implemented. MAC functions are normally implemented in Software running on general purpose processors. This way changes can be made easily by changing the software. The PHY usually contains high-speed digital and analog circuits and is usually designed in dedicated hardware because it the signal rates are faster than general purpose processors can process the data. Hardware is used when precise timing and short response times

are needed. The problem is that hardware changes require the ASIC to be redesigned, which is a long and costly process.

In this invention, Logvinov teaches that the logical lower part of the digital MAC that runs fast can be physically implemented in hardware called the "HardMAC" and physically combined with the top digital part of the PHY function. The term "SoftMAC" (software MAC) can be used to described the portion of the MAC implementation that continues to run on the processor as before. Putting MAC functions in hardware improves performance such as precision timing and short response times, but exposes the chip to higher risk due to changes in the design or regulatory needs. Logvinov resolves this issue by pre-defining the typical functional blocks needed by the communications system, and made their parameters programmable. For example, the pre-defined function of the Forward Error Correction hardware block calculates a Cyclic Redundancy Check (CRC) number. The specific polynomials used in the calculation can be programmed into the hardware block by the coprocessor. This has the advantage of keeping the MAC and PHY layer very flexible, and at the same time keep it capable of high speeds and precision timing.

Regarding the rejection of Claim 1, Schaeffer, JR. et al ("Schaeffer") claims a very flexible MAC/PHY layer in his citation: "media access controller/physical interface (MAC/PHY) 14". As explained above, Logvinov solves the MAC/PHY performance and flexibility problem with the novel concept of the splitting the software and hardware MAC to create the HardMAC implemented in hardware and whose parameters are programmed by the module's coprocessor. Logvinov's flexibility is in the context of a flexible pre-defined hardware design. Schaeffer has no concept of how the MAC/PHY are physically implemented or the advantages of splitting

them into soft and hard components and therefore does not recognized the problem being solved by Logvinov.

In Schaeffer, "a single MAC/PHY integrated circuit is capable of providing its service for multiple data ports", [0071]. This refers to the ability to use one MAC/PHY to support several communication links. He is not referring to the hardware programmability flexibility in the context of Logvinov.

Schaeffer also says, "The MAC/PHY 14 is an industry standard processor that is capable of preparing data signals for transport onto powerlines, and 2 receiving data signals that have been transmitted via powerlines", [0057] and fig. 13". The "industry standard processor" mentioned here is the main system processor for running the software MAC including receiving and sending data. In Logvinov, this more closely corresponds to the "general purpose processor" 100 in figure 1. The coprocessor 200 in figure 2 described by Logvinov is dedicated to controlling the pre-defined function blocks 210-245, which is the coprocessor in claim 1 and is very different from Schaeffer's "industry standard processor". In fact, by claiming only a general purpose processor and not a coprocessor that controls pre-defined hardware blocks, Schaeffer teaches away from the split hardware/software MAC taught by Logvinov.

Regarding Claim 2, as presented by the Examiner, Logvinov claims the hardware module can be easily adapted to changes in regulatory but Schaeffer indicates "security is an excellent application of the technology [0092]" and "....ability to adapt to protocols in order to transport useful data. Consider the subject of what will be discussed hereinafter as common protocols, cross protocols and native protocols, [0101]". It is true that both Loginov and Schaeffer claim

simple protocol changes by simply changing the programming. However, Schaeffer's intentions are at the application level and above the MAC using a "protocol translator' (Claim 3, Line 3). Logvinov is claiming that his flexibility is specifically due to the design of the ASIC with the HardMAC that prevents the need to remake the chip due changes in regulations, applications or protocols. Schaeffer does not anticipate the problem solved by Logvinov.

Dependant Claims 3, 5 and 6 are considered valid, because the independent claim has been responded to above.

Dependant Claim 4 is considered valid for the same reason.

The reference to Kostoff is noted. It limits the loss of bandwidth due to flow control issues, e.g. the lack of a response that a transmitted signal was received. The solution proposed by Kostoff may have a faster response to the protocol messaging. Logvinov's speed improvements come from the implementation of MAC functions into hardware (HardMAC). These are two completely different concepts and therefore Kostoff does not suggest the solution invented by Logvinov.

The Examiner is respectfully requested to withdraw the rejections under 35 U.S.C. § 102(b)

IV. 35 U.S.C. § 103(a)

Dependant Claim 4 was rejected as being unpatentable over Schaeffer, JR. et al. further in view of Ashlock. Since the independent claim has been responded to above, the Examiner is respectfully requested to withdraw the rejections under 35 U.S.C. § 103

V. Conclusion

This response attends to each point noted by the Examiner. Claims 1-6 currently pending in this case are proper and patentable. Allowance is respectfully requested. However, should the Examiner deem that further clarification of the record is in order, we invite a telephone call to the undersigned prior to the issuance of the next office action to expedite further processing of the claims to allowance.

Respectfully submitted,

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